M114 DUAL CV-GATE DELAY

FUNCTION DESCRIPTION

The M114 DUAL CV-GATE DELAY is one of a kind module in the family. It features 2 channels that store incoming CV and GATE signals and bring them back with an adjustable delay from 2msec. up to 10 sec.

Both incoming CV and GATE signals are stored every 1msec in 5 separated 10000 bytes chunks to a 65536 bytes SRAM. Like any delay processors the incoming datas are first stored in memory then read back after a determined delay. Incoming GATE pulses need to be 3.5v peak min. GATE outputs are direct timed copies of what was stored at GATE's inputs (4.5v peak pulses). Both CV's ranges are from 0v to +8v. CV's outputs will be a direct copy of what was stored at CV's inputs.

The ADC/DAC conversions are made using 2 small custom made 16 bits SIP modules mounted on the main board and read by a Microchip PIC microcontroller.

The printed circuit board

The module uses a 2U Moog style front panel. The PCB is a double side board, 2.8" X 5.5", has 4 mounting holes, one on each corner and is mounted on 4 x 4-40 1/4" "standoffs. All the parts are through hole types.
Connectors P1 to P3 are positioned to be adjacents to their dedicated pots.
100kB lin potentiometers are used for smooth delay response.
Power is connected by use of a 6 pins 0.156" Molex type connector.
All the wiring cables are hookup wires type.

The circuit description

The M114 DUAL CV-GATE DELAY circuitry is mostly digital.
Here is a description of one of the 2 available channels:

All the memory read/write are managed by U6 which is a Microchip PIC16F1783.
The software uses an 'interrupt based' logic to access all
the devices and make the appropriate delays.
And all the logic exchanges between the ADC's, DAC's and SRAM's
are made through SPI serial communication.

ADC-DAC SIP module

H3 & H4 are both 16 bits ADC/DAC SPI converters mounted
on small 15 pins SIP pcb's. The circuitry design of these small
SIP converters was made possible with the help of a European engineer named
Roman Sowa who agreed to help in my design process.
He helped making the converters do their jobs
with a maximum of precision and in a noise free pcb layout.
The incoming CV is connected to H2 through the CV input jack.
Then the 0-8vdc incoming voltage is precisely dropped to 0-5vdc using
a voltage divider made of 0.1% precision resistors R1,2,3. The voltage is then
buffered by U3 which is a **OPA990** precision opamp. The buffered voltage is then
fed to U1 which is a **MAX11100EUB+** precision 16 bits ADC. The ADC data is read
through SPI communication to the PIC. The SRAM stored data can be read back by
the PIC and sent to U4 which is a **LTC2641CMS8-16#PBF** precision 16 bits DAC.
The 0-5v data needs then to be amplified back to 0-8v.. This is done using
another **OPA990** precision opamp (U5) with the necessary gain setup with
resistors R8,9,10,12. H3 connector send the final CV to the CV output jack.

The main board

P1 & P2 potentiometers are used to set both delays and are explained below..

Both GATE inputs are managed through Q2 & Q4 who act as inverter buffers
to bring 0-5v pulses to the PIC micro. The stored GATE data are then read back
and sent to Q1 & Q3 that also act as inverter buffers to bring the GATE pulses
polarities similar to the originals.
The memory used for data storage is a 64k x 8 bits SPI based SRAM 23LC512 (U7).

Memory addresses mapping (5 x 10000 bytes chunks):

0-9999 are for GATE1 & GATE2 data (bit0:GATE1 bit1:GATE2).
10000 to 19999 are for CV1 (ADC/DAC 8bits MSB)
20000 to 29999 are for CV1 (ADC/DAC 8bits LSB)
30000 to 39999 are for CV2 (ADC/DAC 8bits MSB)
40000 to 49999 are for CV2 (ADC/DAC 8bits LSB)
50000 to 65535 not used

Each of the first 5 sections have 10000 bytes memory spaces.
Using a 16 bits TIMER an interrupt function is called every 1 msec.
A minimum of 2 addresses read/write (2msec.) and a maximum of 10000 addresses
read/write (10sec.) can be done depending on the dialled delay.

For example the following interrupt sequence is made every 1msec:

- Read GATE1 data from actual SRAM address (0-9999, bit0)
- Output stored data to GATE1 output jack
- Read CV1 voltage data from SRAM address (10000-29999, 16 bits)
- Output stored CV1 voltage to CV1 output jack
- Store GATE1 input signal state to SRAM address (0-9999, bit0)
- Store CV1 input voltage (ADC1 conversion) to SRAM address (10000-29999)

- Read GATE2 data from actual SRAM address (0-9999, bit1)
- Output stored data to GATE2 output jack
- Read CV2 voltage data from SRAM address (30000-49999, 16 bits)
- Output stored CV2 voltage to CV2 output jack
- Store GATE2 input signal state to SRAM address (0-9999, bit1)
- Store CV2 input voltage (ADC2 conversion) to SRAM address (30000-49999)

The memory spans depends on the dialled delay value from 2msec. to 10sec.
The delay pots are read by the PIC micro and will give a value from 0 to 255.
These 256 values are indexes of a look-up table that contains
the exact 16 bits delay values needed to track the front panel layout
delay duration. For example the delay pot#1 positioned at 1 sec.
will be read as around middle of 256 or 128. In the delay look-up table,
the index value of 128 will hold a 16 bits value of 1000 which stands for
1000 msec or 1 sec. In this example a counter from 0 to 1000 will be increment
every interrupt of 1msec from 0 to 1000 then rolls back to zero and continue.
The address sweep always start from 0 to the dialled delay (up to 10000).

Both channels ADC’s & DAC’s CV voltages are accurate within +/-1 LSB
and are an almost perfect copy of the incoming CV’s.
This keeps pitches of both input and output tracking correctly.
Both CV’s ranges are from 0v to +8v. CV’s outputs will be a direct copy of what
was stored at CV’s inputs.

No Adjustments or trimmings required.

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ELECTRONIC SPECIFICATIONS

POWER CONNECTOR PIN ASSIGNMENTS	
1	−15V
2	A GND
3	A GND
4	+15V
5	D GND
6	+5V

Panel Size: Single width 2.125”w x 8.75”h..
Number of channels: 2
Each channel controls:
Delay pots: 2msec. to 10sec.
GATE input-thru impedance: >100k
GATE input pulse level: 3.5 volts peak min.
GATE output impedances: 1k ohms +/-5%
GATE output pulse level: 4.5 volts peak.
CV input-thru impedance: 100k +/- 0.1%
CV input range: 0 to +8v
CV output impedances: 300ohms +/-5%
CV output range: 0 to +8v

Power:
+15V @ 1mA,
-15V @ 1mA,
+5V @ 80mA max.